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In situ observation of electrode melting in multilayer ceramic capacitors

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In the usage of multilayer ceramic capacitors, we are concerned with the intrinsic dielectric properties of the ceramic and its long-term stability/reliability under external stresses in service conditions. Of equal importance to long-term reliability is the short-term survivability under current (power)-surge conditions. It differs from the ability to withstand voltage surge, which is determined by the dielectric strength of the ceramic. In this paper, we present some observations on sectioned and polished multilayer ceramic capacitors, which were subjected to "controlled" current-surge test conditions. Capacitors from several vendors were examined. The samples were examined *in situ* under an optical microscope while current pulses of varying magnitude were applied at a constant voltage. Subsequently some samples were further examined by scanning electron microscopy. The failure mechanism appeared to be the heat-induced local melting of internal electrodes, which might then lead to a blow-out or charring of the capacitor. In less severe cases, we observed local melting and crack formation in the surrounding ceramic as well. The primary change in capacitor properties was in the degradation of the insulation resistance. In severe cases, this also led to an increase in the dissipation factor.

1. Introduction

In the manufacture of multilayer ceramic capacitors (mlc), we are concerned with the intrinsic dielectric properties of the ceramic and its long-term stability/reliability under external stresses in service conditions. Studies on commercial mlc [1, 2] have established a voltage coefficient of approximately 3 and an apparent activation energy of 1 eV, based on the usual reliability model [3].

Of equal importance to long-term reliability is the short-term survivability under current(power)-surge conditions. This differs from the ability to withstand voltage surge, which is determined by the dielectric strength of the ceramic. For protection against current surge, the Electronics Industry Association (EIA) recommends a current-surge test at 2.5 times the rated voltage, with a charging currrent not exceeding 50 mA. In actual circuits, it is not uncommon that capacitors encounter current transients as high as 2 to 3 A. Those that fail the large current surges are generally charred and short-circuited.

At the present time, the failure mechanism of the current-surge test is not understood. It is even more difficult to pin-point the cause(s). Current-surge failures might be due to some extrinsic defects introduced into the mlc body during various stages of processing, similar to delaminations or large voids being associated with infant mortality failures in accelerated life tests. Or the surge failures might be due to some intrinsic materials properties, similar to the motion of oxygen vacancies in the ceramic contributing to long-term reliability problems. In this paper, we report a simulated current-surge test on sectioned and polished mlc samples. We observed *in situ* the surge failures taking place.

2. Experimental procedures

The mlc samples were mounted using the typical metallurgical (cold-mount) techniques. They were first polished with 320 mesh paper, with final polish using 0.05 μm alumina powder. Each sample was photographed under an optical microscope to obtain an initial feature map. Then it was subjected to a "controlled" current-surge test.

We simulated the current-surge test at a constant voltage by varying an external resistor, resulting in different amounts of current being delivered to the sample. The voltage was fixed at 125 V in this study, which was 2.5 times the rated voltage of 50 V. The current was delivered in shots varying from 40, 125, 500 mA and 1 A and lasting for a few seconds. The Appendix gives a derivation of the maximum surge current and the duration. The sample surface was monitored through the optical microscope during each current shot to see if any changes had occurred. When the capacitor failed the current-surge test and became electrically short, it could no longer substain a voltage and the voltage across the sample dropped to zero. The experimental set-up is shown in Fig. 1.

Four lots of mlc from several vendors were examined: α, γ, β and δ, with a nominal capacitance of 0.1, 0.1, 0.33 and 0.1 μF, respectively. The chip bodies (excluding encapsulation) had the same dimensions of 0.090 in. × 0.050 in. × 0.50 in. The number of internal electrodes differed: 16 for lot α, 25 for lot γ, 47 for lot β and 41 for lot δ. The average dielectric thickness was

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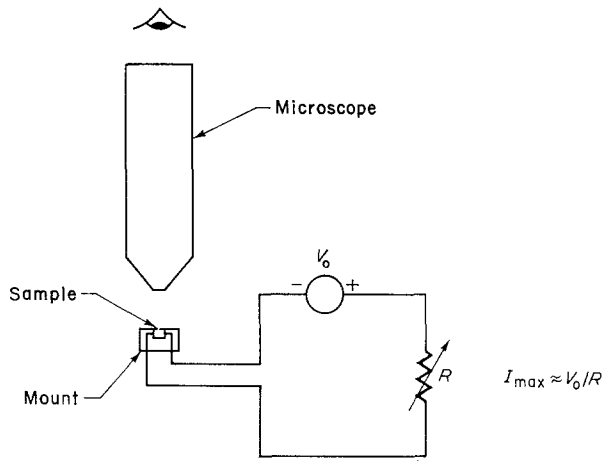

Figure 1 Experimental set-up in this study.

measured to be 0.0009 in. (22 μm) for lots α, β and δ, and 0.0012 in. (30 μm) for lot γ. All the samples were measured to have the proper values of dissipation factor (DF, or tan δ) so that they were good samples to begin with. After the current-surge test, some samples were further examined by scanning electron microscopy (SEM).

3. Results and discussions

A general observation from this study is that the initial microstructure in the polished plane of the sample did not indicate whether the sample was more prone to surge-test failure. Fig. 2 contrasts two samples from lot γ: (a) shows a normal mlc cross-section, except for several pockets of thick internal electrode, while (b) shows a large delamination near the cover layers. The latter sample also had seen more poishing such that several electrode layers had disappeared completely. Both samples passed the current surge test at the maximum applied current of 1 A.

When changes occurred during the current-surge test, it could be in the form of local electrode melting, a small blow-out or complete charring. Obviously, the severity of damage depends on the maximum current applied, defined as I_{max}. When complete charring of the sample occurs, it was usually preceded by a flash of bluish colour, indicating very high temperature in a short duration. Furthermore, an event such as electrode melting did not seem to occur between electrodes with the narrowest spacing. The following sections describe the observations on the four lots of mlc in sequence and Table I lists all the samples used in this study.

3.1. Lot α

On the first sample, no change was observed both electrically and microstructurally until I_{max} was increased to 500 mA, when a dark line appeared along an electrode–ceramic interface. In the second sample, we purposely gave a few more shots at 500 mA, but we did not notice any changes. When I_{max} was increased to 1 A, the capacitor charred and became electrically shorted. The third sample proved to be more revealing in the current-surge phenomenon.

Fig. 3a shows the initial microstructure prior to the surge test. The mlc contained many internal distortions, including large delaminations, distorted and bent electrodes as well as microcracks. Such defects were not observed in the first two samples. After a few shots of current pulses at I_{max} = 40 mA were applied, we began to notice localized electrode lines turning black in the optical microscope. As more shots at the same current level were delivered to the sample, the darkened electrode lines propagated in length and new regions of darkened electrodes appeared. Fig. 3b shows the microstructure after the test. There were four areas where the electrode lines had turned black. While the darkened lines occurred near the large delaminations, they did not extend to the full length of the delaminations. Furthermore, the largest area (marked A) extended away from the delamination and covered nine electrode layers. It was not clear whether the delaminations in this sample in some way induced the electrode-darkening phenomenon.

Scanning electron micrographs of this sample are shown in Fig. 4. Both Figs 4a and b were taken in the back-scattered electron mode of the SEM while Figs 4c to f were taken in the secondary electron mode to give a better contrast in the images.

Figs 4b and c focus on the same area, A, previously shown in Fig. 3b. The as-polished electrode lines were flat and smooth while the appearance of the darkened electrode lines indicated that melting and re-solidification of the electrodes had taken place. This region is shown in higher magnifications in Figs 4d to f. Energy dispersive X-ray (EDX) analysis of the electrode area

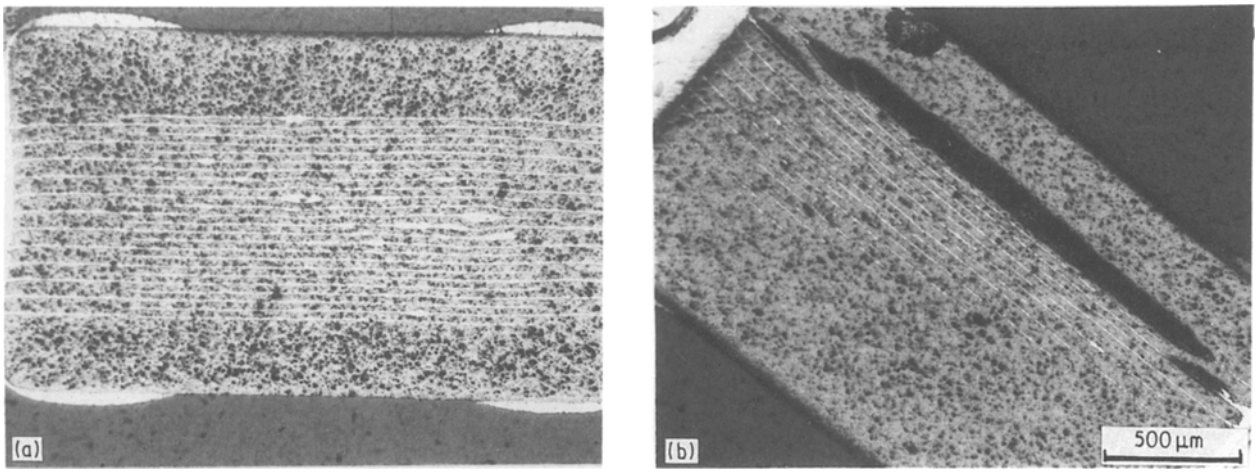

Figure 2 Cross-sections of two different samples in lot γ.

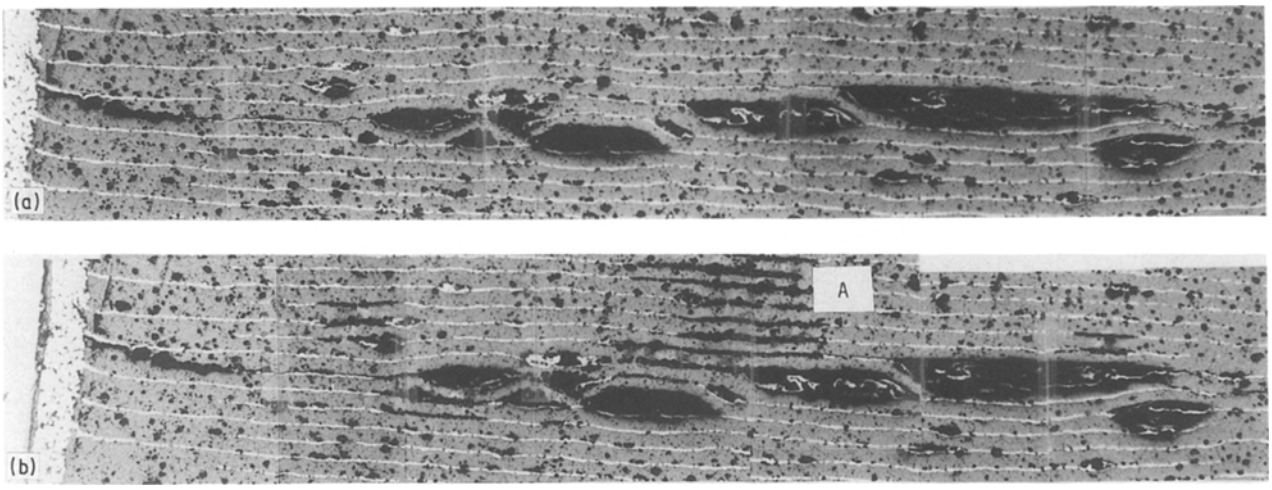

Figure 3 Optical micrographs of lot α, sample 3: (a) before surge test, and (b) after surge test.

in Fig. 4f revealed silver (Ag) and palladium (Pd) peaks. No other peak with significant intensity was detected. This suggested that very little, if any, inter-diffusion between the ceramic and metal electrode took place during the brief high-temperature event. Oxygen was most likely present together with the metals, because the Ag/Pd were probably oxidized to give the dark appearance in the optical microscope. However, our SEM was not able to detect elements with an atomic number as low as oxygen. In Fig. 4e, the shape of the ceramic bordering the electrode also pointed to a melting and re-forming of the ceramic in that area.

3.2. Lot β

Two samples were subjected to current pulses increasing up to 500 mA without any observable damage optically or electrically. For the next two samples, I_{max} was further increased to 1 A. Both failed and charred at that current level. For the fifth sample, small regions of darkened electrodes appeared when I_{max} was increased to 500 mA. Simultaneously, a bluish flash was observed in the optical microscope whereby a dark void covering eight electrode layers were formed. These features are shown in Fig. 5a. A higher magnification of the void border (Fig. 5b) shows some large cracks induced by the void formation. The capacitor also became electrically shorted.

Sample 5 was slightly re-polished and then examined in the SEM. Figs 6a to e show increasingly higher magnifications of the void area. The slightly whitish areas bordering the void (marked by arrows in Figs 6b and c) indicated melted and re-solidified electrodes. On the inner wall of the void, we found hemispherical particles which were identified by EDX to be droplets of Ag/Pd (Fig. 6e). In this sample, we unambiguously observed electrode melting due to the current-surge test, which eventually led to a minor blow-out in the capacitor.

3.3. Lot γ

In two out of the three samples we examined in this lot, we did not detect surge-test failure up to I_{max} = 1 A. On sample 3, an I_{max} of 40 mA caused the appearance of three darkened electrode lines (Fig. 7b) in an area where none was observed initially (Fig. 7a). As more shots of 40 mA were delivered to the sample, the dark lines grew in length and two additional neighbouring lines were affected (Figs 7c and d). The capacitor still maintained good DF and insulation resistance (IR) values.

We decided to re-polish the sample to determine the extent of damage. Fig. 8a shows area A before re-polishing. After removing about 0.001 in. (25 μm) of the surface, an expanded view of area A is shown in Fig. 8b. The damaged electrode layers were mostly removed except for a deep hole and a small stretch of

TABLE I Mlc samples examined in this study

Lot	$C(\mu F)$	$t(\mu m)$	Sample	I_{max} (mA)	Comments
α	0.1	22	1	500	dark crack along electrode/ceramic interface
			2	1000	charred
			3	40	electrode melting
β	0.33	22	1	500	no damage
			2	500	no damage
			3	1000	charred
			4	1000	charred
			5	500	electrode melting, void formed
γ	0.1	30	1	1000	no shorting or visible damage
			2	1000	no shorting or visible damage
			3	125	electrode melting, IR degradation
δ	0.1	22	1	1000	no damage
			2	1000	no damage
			3	40	darkened electrode

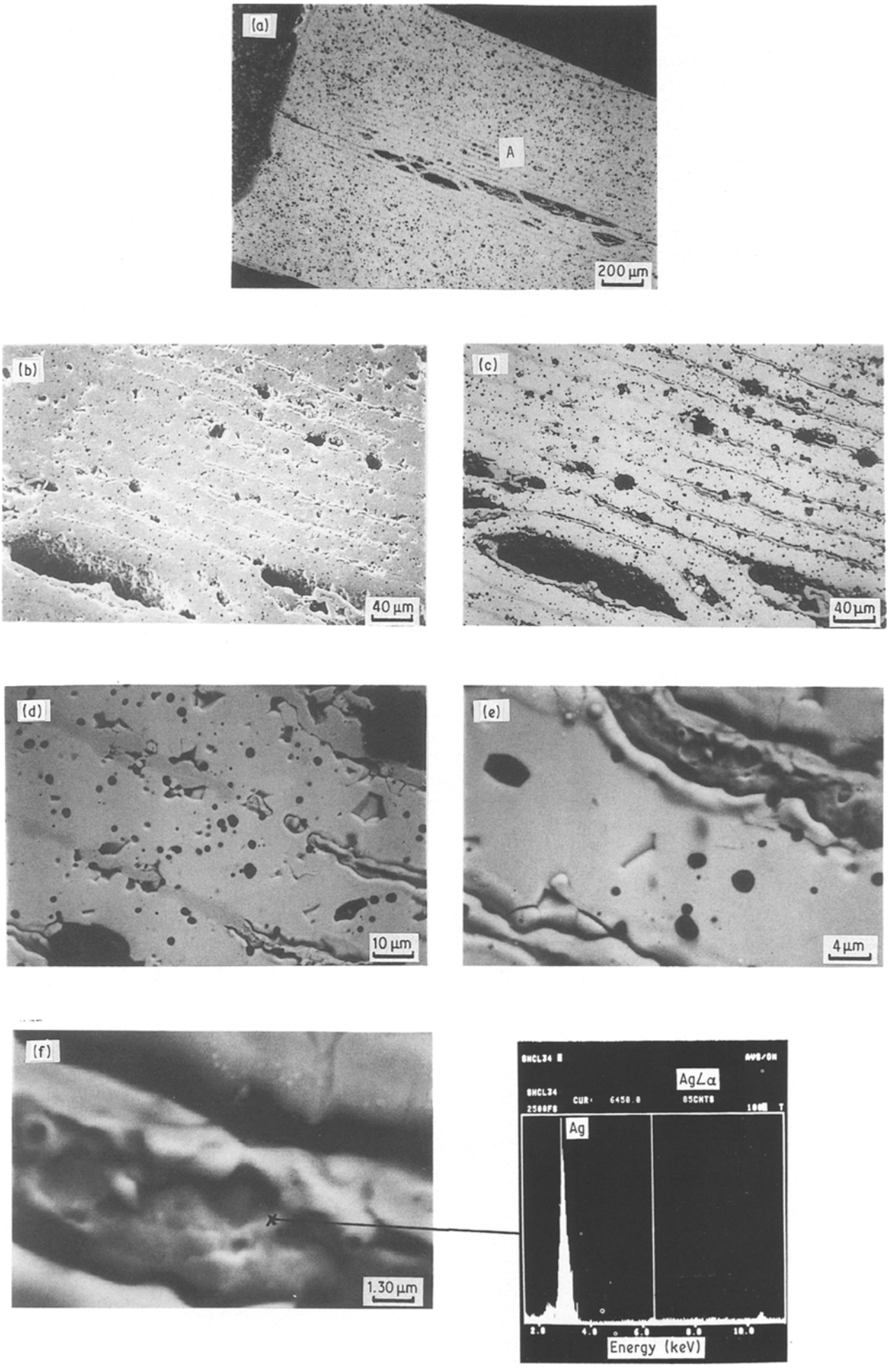

Figure 4 Scanning electron micrographs of the sample in Fig. 3b showing melted and re-solidified electrodes.

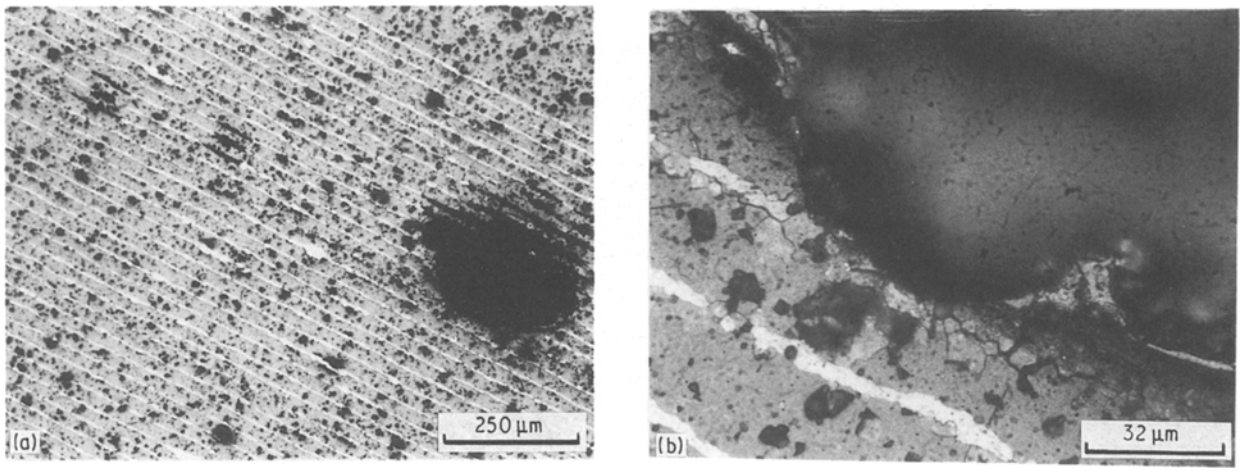

Figure 5 Optical micrographs of lot β, sample 5, after surge test showing (a) a large void and several regions of darkened electrodes, and (b) cracks near the void.

melted electrode (marked by an arrow). However, two additional areas, B and C, were found to contain some damage not seen prior to the re-polishing. The capacitor still maintained its initial values of capacitance of 0.0784 μF, a DF of 1.36% and an IR of $2.5 \times 10^{10}\ \Omega$.

When one more shot of 40 mA was applied to the re-polished sample, darkened electrodes appeared in areas B and C (Fig. 8c). The surrounding ceramic also showed bluish coloured burnt mark, as indicated in Fig. 9. The capacitance increased to 0.0837 μF, DF to 1.75% while the IR decreased to $1.7 \times 10^9\ \Omega$. Subsequently, another six shots of 40 mA and six shots of 125 mA current pulses were delivered to the sample with no further visual changes. The properties remained the same, with a capacitance of 0.0839 μF, a DF of 1.70% and an IR of $2.5 \times 10^9\ \Omega$. After the sample was left overnight, both the capacitance (0.0796 μF) and the DF (1.28%) returned to the initial values prior to testing, but the IR remained at the degraded value of $1.5 \times 10^9\ \Omega$. Thus the temporary change in capacitance and DF appears to have been caused by the heat generated during the surge test, but the degradation in IR is permanent. When the IR

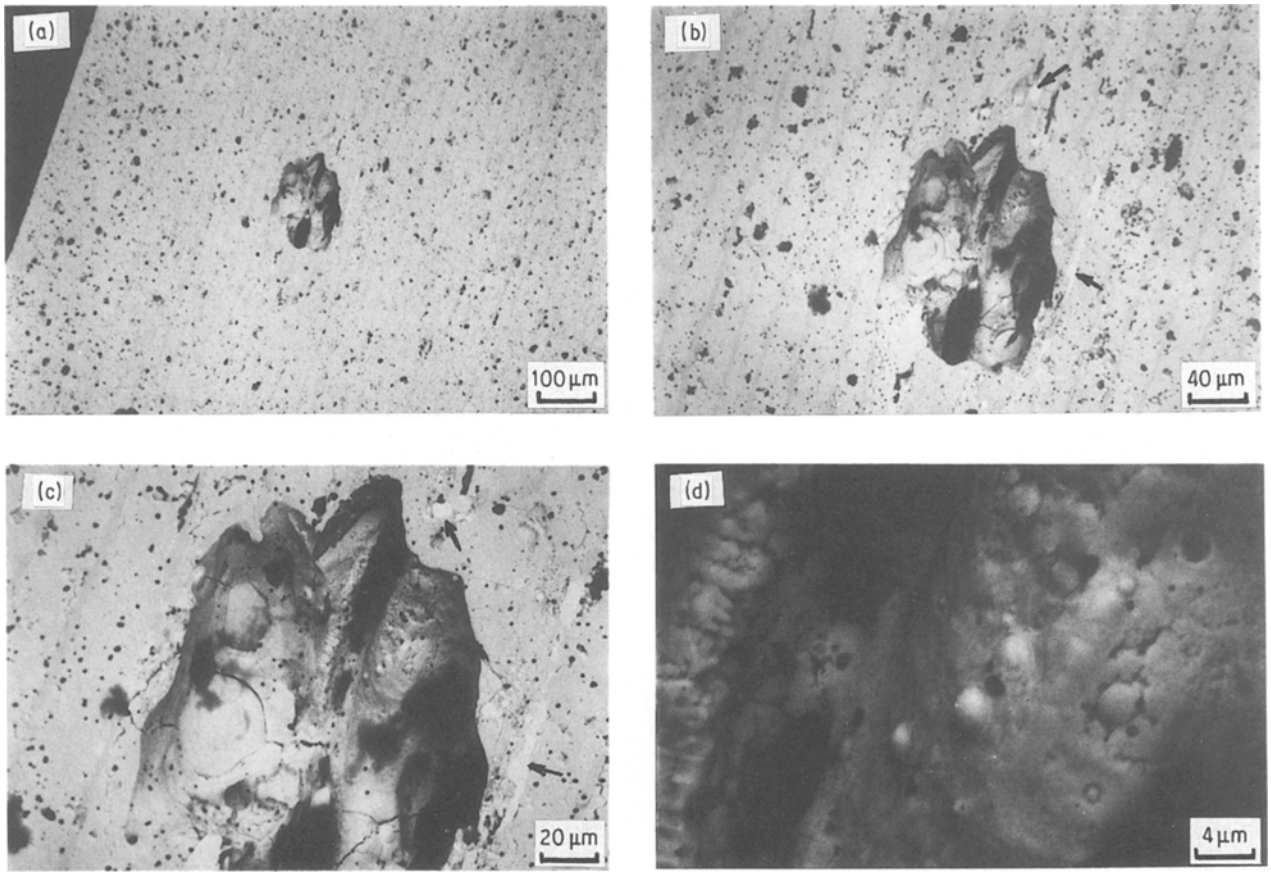

Figure 6 Scanning electron micrographs of the void in Fig. 5, showing (a) the void, (b) melted electrodes, (c) cracks, (d) hemispherical droplets of Ag/Pd and (e) a hemispherical particle of Ag/Pd and magnesium-rich inclusions together with the EDX analysis.

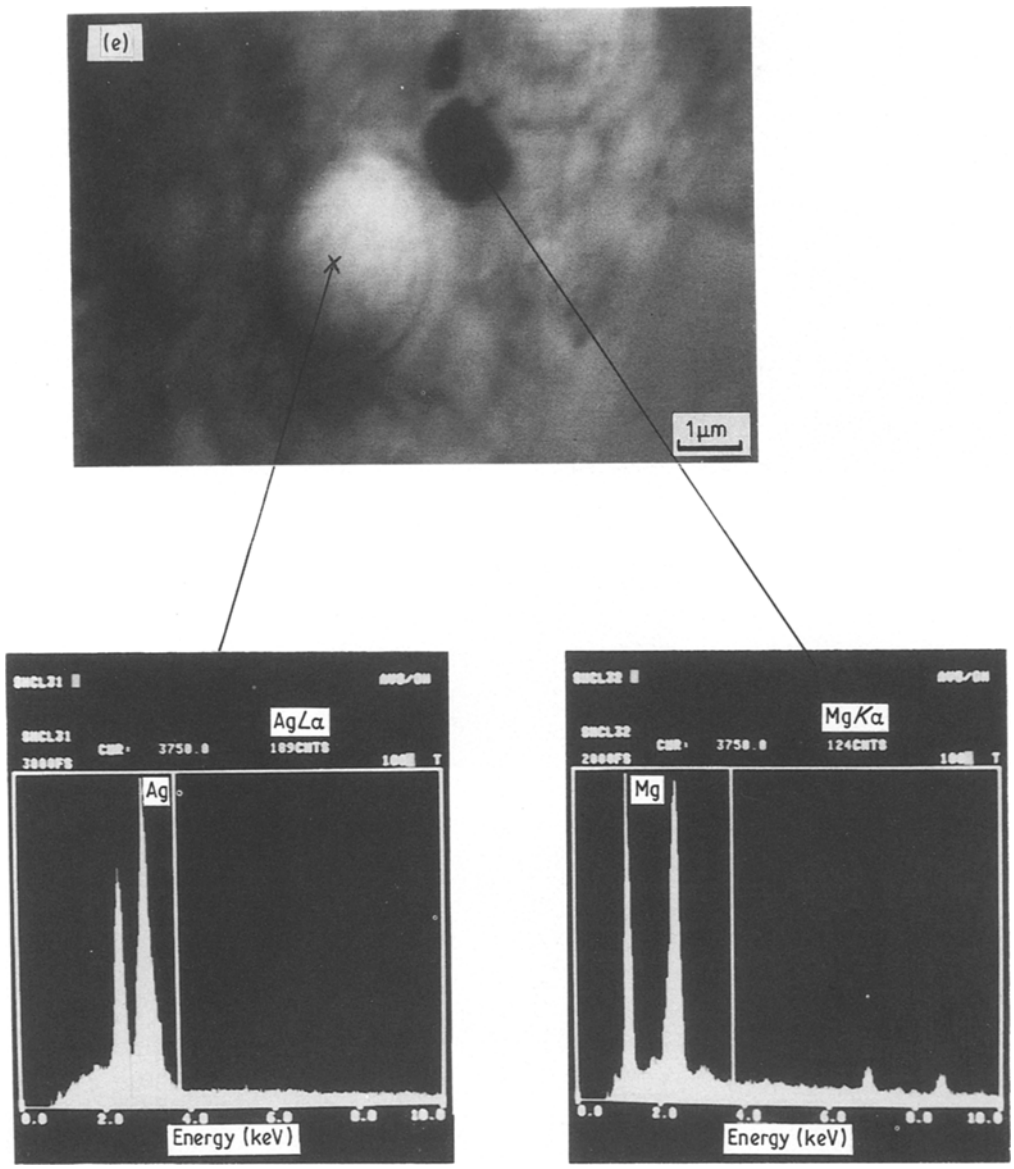

Figure 6 Continued.

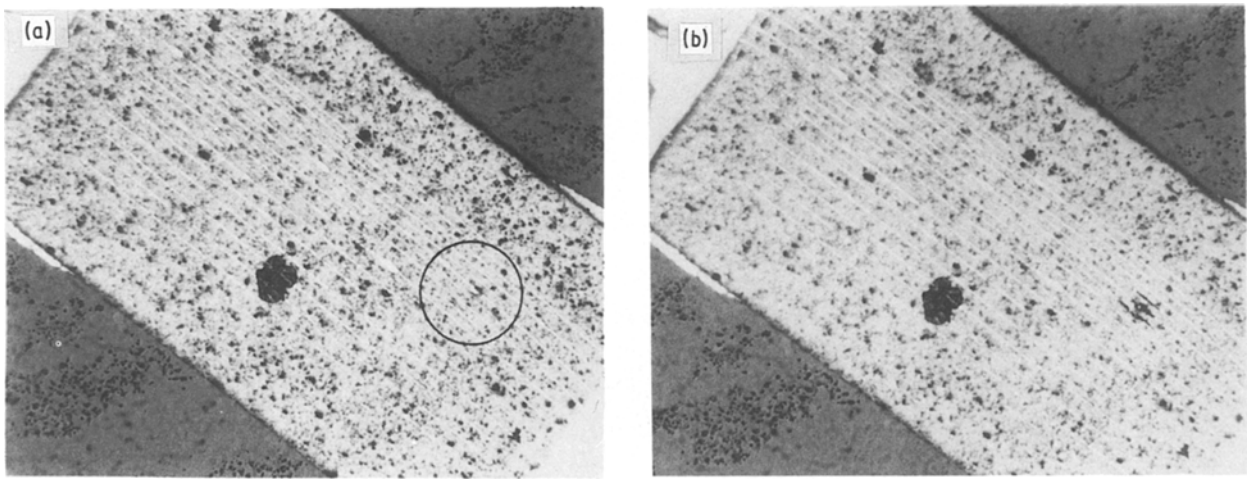

Figure 7 Optical micrographs of lot γ, sample 3: (a) before surge test, (b) after one shot of 40 mA current, (c) after further shots of 40 mA current, and (d) after additional shots of 40 mA current.

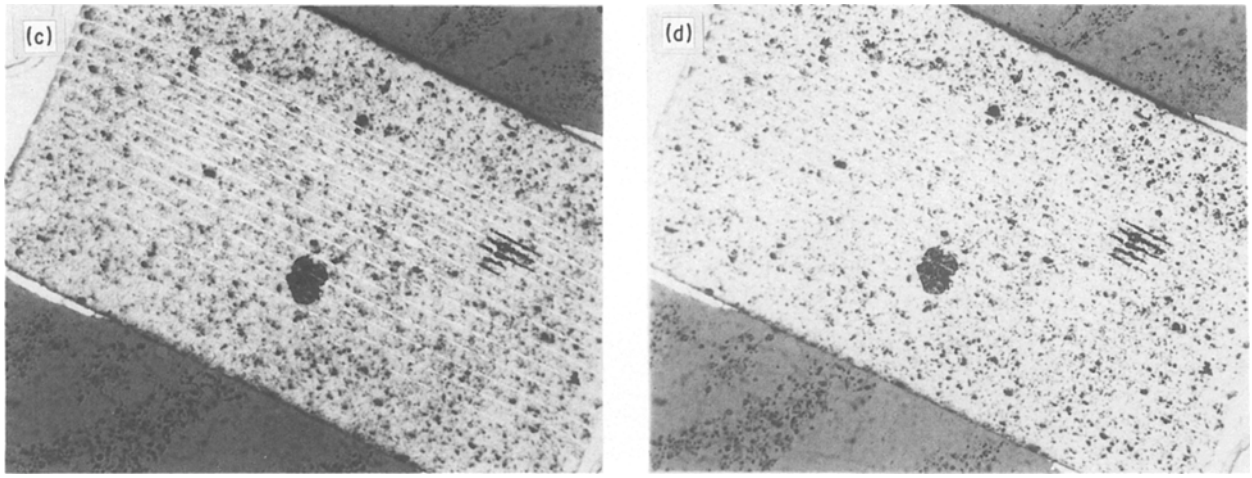

Figure 7 Continued.

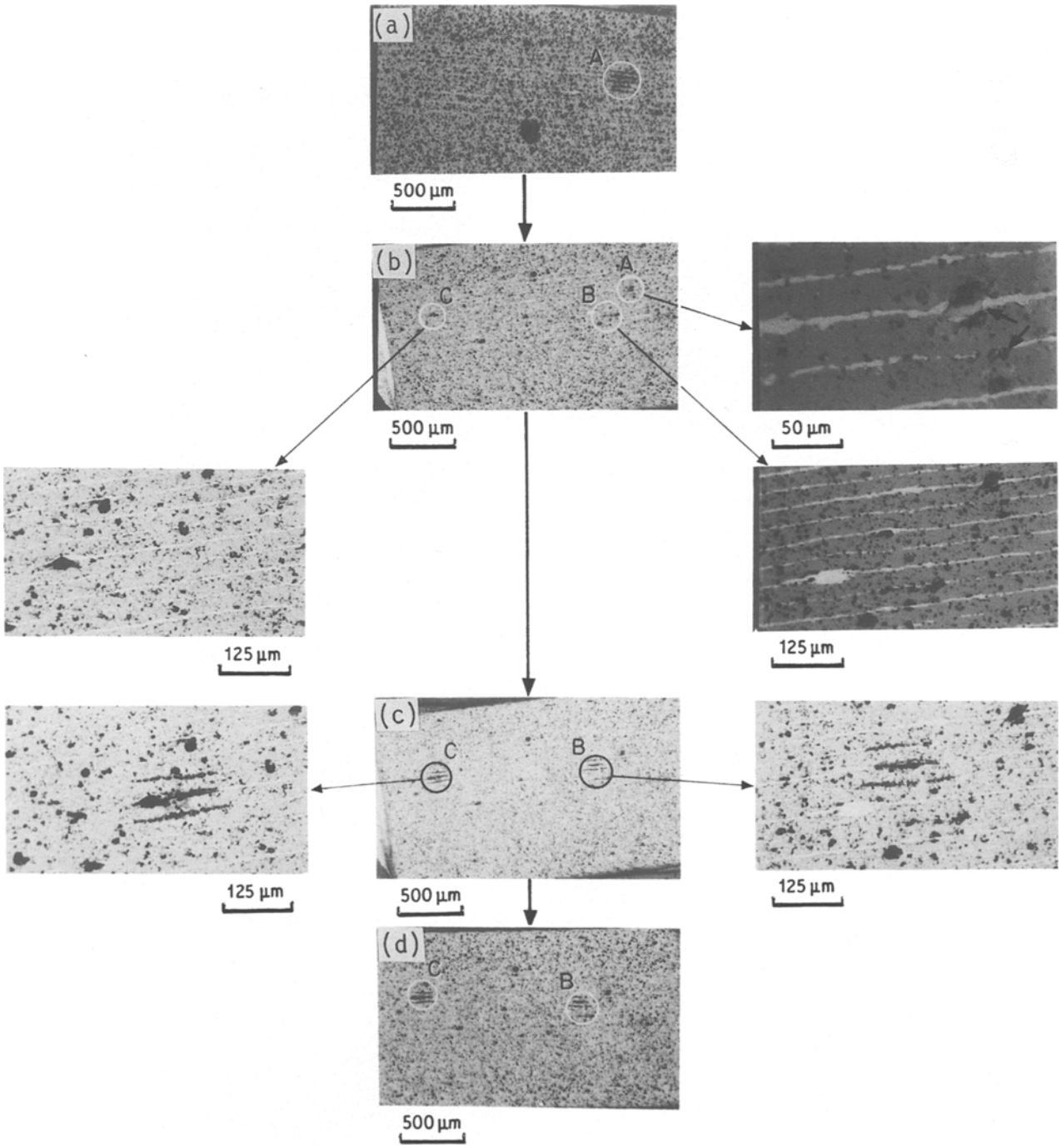

Figure 8 Optical micrographs of lot γ, sample 3: (a) after the test described in Fig. 7, (b) re-polished to remove 0.001 in. (25 μm) from the surface, (c) after one more shot of 40 mA current, and (d) after six shots of 40mA and six shots of 125 mA current.

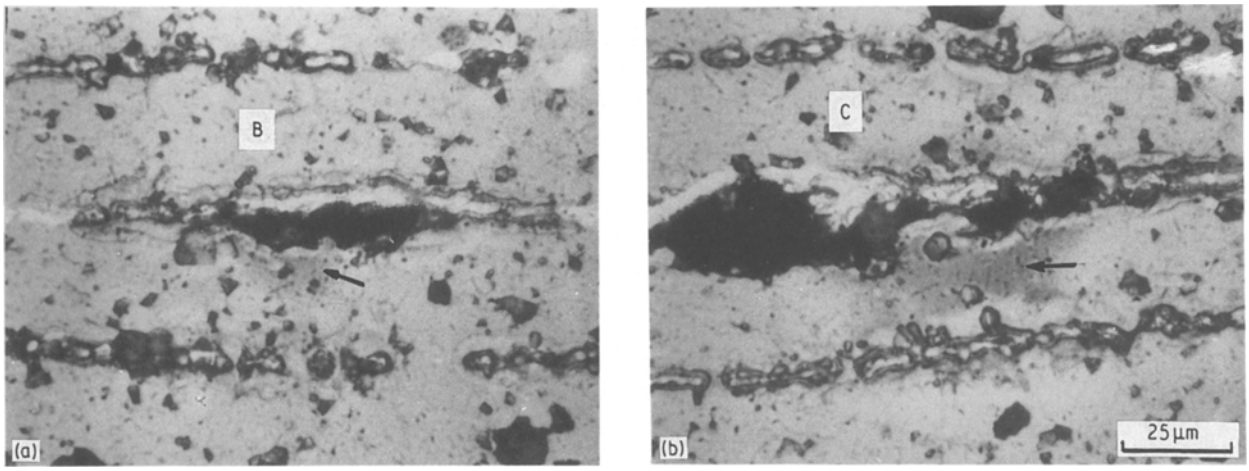

Figure 9 Higher magnifications of areas B and C in Fig. 8d to show the burnt marks in the ceramic.

degradation becomes so severe that its contribution to the DF dominates [4], DF will also be permanently degraded.

3.4. Lot δ

In this lot, one out of three samples tested suffered damage as a result of the current-surge test. After polishing, the sample had a capacitance of 0.0633 μF, a DF of 0.93% and an IR of $1.7 \times 10^{10}\,\Omega$. After five shots of 40 mA current, two separate areas of darkened electrodes were observed, with some burnt marks in the neighbouring ceramic. This is shown in Fig. 10. As in the case of lot γ, the capacitance increased to 0.070 μF, DF to 2.06% while the IR dropped to $1.7 \times 10^{9}\,\Omega$. After waiting for 24 h, both the capacitance and the DF were restored to the initial values, but the IR degradation remained.

3.5. General discussion

Observations from the present study can be generalized as follows. When a polished sample is subjected to the current surge test, it might experience

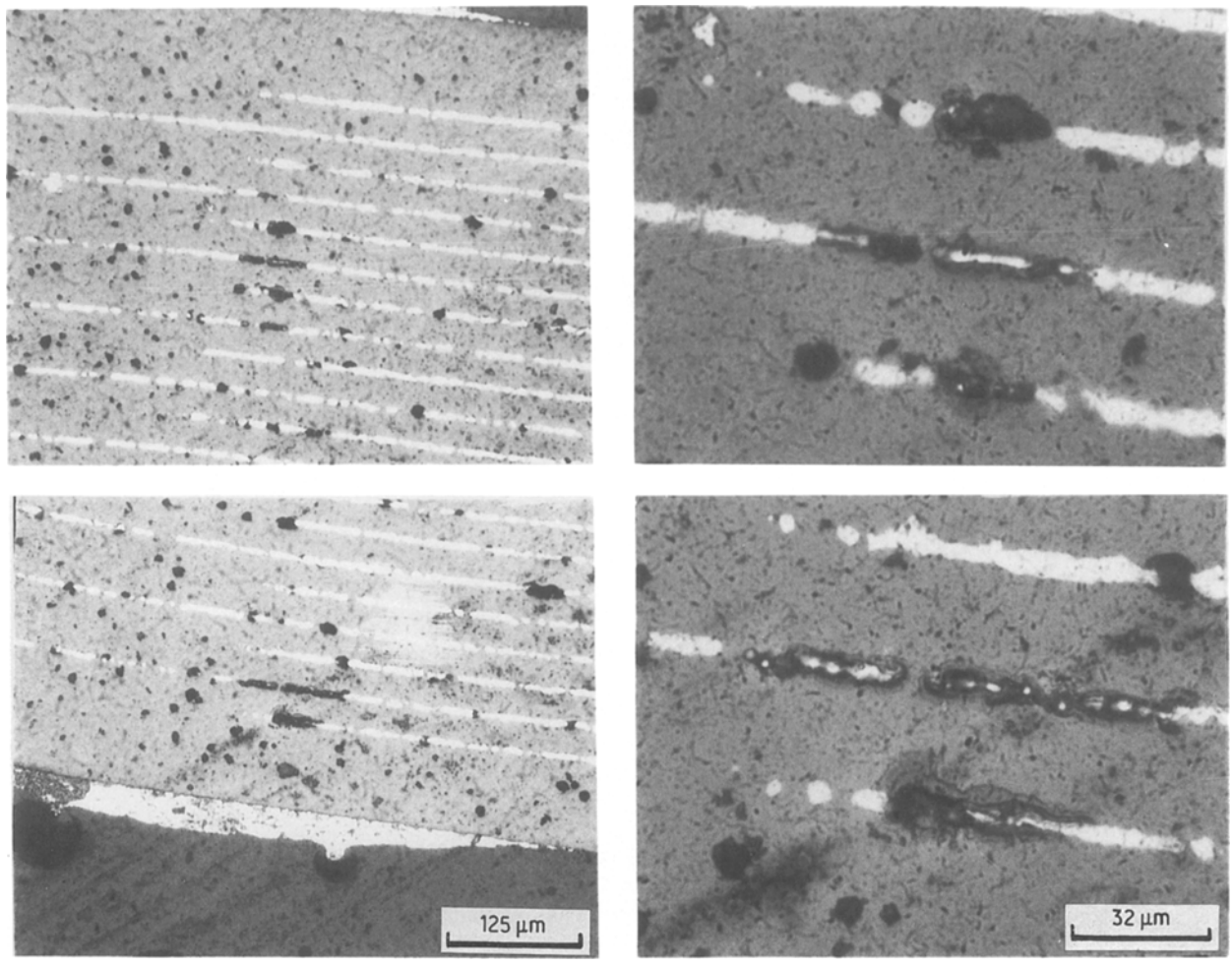

Figure 10 Optical micrographs of capacitor from lot δ after surge test, showing two areas of darkened electrodes.

(a) no electrical short or surface damage,

(b) electrical short but no surface damage,

(c) electrical short with large void formation; in severe cases, it leads to charring of the capacitor,

(d) electrical short or IR degradation with darkened electrode lines caused by melting and re-solidification and oxidation of the electrode metals.

All the damage we observed in the samples occurred far away from the termination interface. This rules out high contact resistance between the termination and the internal electrodes as the cause for failure. A simple calculation also demonstrated that resistive (joule) heating due to the sheet resistance of the internal electrodes is much too low to cause the melting of electrodes. One issue worth more discussion is the possibility of voltage breakdown between the electrodes exposed to air by polishing.

Previously, both experimental [5] and theoretical [6] studies on high-voltage breakdown of electrodes on printed wiring boards have been published. It is known that in general, a metal–insulator–air interface reduces the breakdown voltage. For copper electrodes on epoxy-glass or triazine PWB, the median breakdown voltage varies from 159 to 234 V/mil*. Electrode melting due to voltage breakdown was not reported. In our study, we had a voltage gradient of 139 V/mil across electrodes in lots α, β and δ and a lower value of 104 V/mil in lot γ. The gradient would be higher across narrower electrode spacings. These values are lower than the breakdown voltages reported in the study on PWB. Furthermore, we reported earlier that as a general observation, we did not see electrode melting occurring between narrowly spaced electrodes in our samples. In one case in this study, we were able to find damage below the surface of a sample subjected to several current pulses (Fig. 8b). Further evidence of non-surface related electrode melting came from cross-sectioning of mlc which failed the dry lifetest (85° C, 100 V) and wet lifetest (85° C, 85% r.h., 100 V) [7]. In these samples, circular areas of internal electrodes were found where the electrode layers had disappeared. The surrounding ceramic also exhibited voids, cracks and evidence of having gone through a high-temperature process locally. From these results, we conclude that the phenomenon of electrode melting seen in this study was not induced by the process of voltage breakdown in air.

Except for the case described in Section 3.3 (Fig. 8c), we were unable to identify visual defects in the polished cross-sections which might be the cause of the melting phenomenon. The chance was very remote from the start that one polished plane would yield such information. It could also be that the defects are on a smaller scale beyond the resolution limit of an optical microscope. It would be beneficial to make mlc with artificially introduced defects, such as voids of well-defined shape and size, to examine further failures resulting from the current surge test. Such model experiments will probably reveal to what extent physical defects play a role in current surge failures.

4. Conclusions

Some observations on sectioned and polished multilayer ceramic capacitors which were subjected to "controlled" current surge test conditions are reported. The failure mechanism appeared to be the heat-induced local melting of internal electrodes, which might then lead to blow-out or charring of the capacitor. In less severe cases, we observed local melting and cracking of the surrounding ceramic. The decrease in the insulation resistance (IR) was the primary degradation in the capacitor properties, until it became so low that the dissipation factor was also affected.

Appendix

The surge-testing circuit diagram is shown in Fig. A1. Initially, the switches S_2 and S_3 are opened and S_1 is closed. This allows the power supply to charge the energy storage capacitor C_1 to a preset voltage level, V_0. Then switches S_1 and S_3 are opened and S_2 is closed, this causes the stored charge (or energy) to be delivered, through the current limiting resistor, R_1, to the sample capacitor, C_2, which is the capacitor to be tested. Because the capacitance of C_1 is much greater than that of C_2, it is eventually charged to the same voltage level as C_1. The peak value of the changing current is limited by R_1. When capacitor C_2 is fully charged, the voltage stays for a preset time interval, then capacitor C_2 is discharged. The discharging cycle starts by opening S_2 and closing S_3. All the charge stored in C_2 is discharged through the resistor R_2. Usually R_1 and R_2 are kept to the same value such that the amplitude and waveform of charging and discharging currents are equal.

The amplitude and waveform of the charging and discharging current pulses can be described as follows. When the capacitor C_1 is charged to the voltage level of V_0, the switch S_2 is closed. The current $i(t)$ flows from C_1 to C_2. Based on Kirchoff's law, this current is described by the integral equation

$$V_0 - \frac{1}{C_1}\int i(t)\,dt = R_1\,i(t) + \frac{1}{C_2}\int i(t)\,dt \qquad \text{(A1)}$$

The solution to this equation can be found in a standard circuit analysis textbook as

$$i(t) = \frac{V_0}{R_1}\exp\left(\frac{-t}{R_1 C}\right) \qquad \text{(A2)}$$

where $C = C_1C_2/(C_1 + C_2)$. Because C_1 is much greater than C_2, therefore C is close to C_2. Assuming

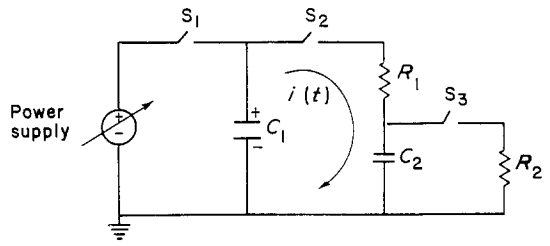

Figure A1.

*1 mil = 2.54×10^{-5} m.

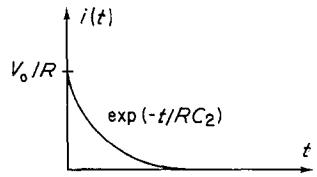

Figure A2.

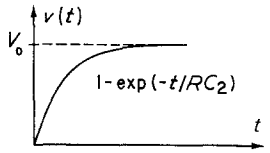

Figure A3.

$R_1 = R_2 = R$, Equation 2 can be written as

$$i(t) = \frac{V_0}{R} \exp\left(\frac{-t}{R C_2}\right) \qquad \text{(A3)}$$

Equation A3 shows the charging current waveform as a function of time. It starts with a peak value of V_0/R and decays exponentially with a time constant of RC_2. The current–time waveform is shown in Fig. A2. If the resistance of the charging resistor R is reduced to zero, theoretically this peak current value can be increased to infinity. However, this is not the case because the inductances of the switch and the resistance of the charging leads will delay the current rising time and suppress the peak value. In this analysis, we have measured that the voltage drop across the charging resistor is much greater than that of the switch and leads during the charging cycle. Experimentally, we have verified the current waveform on an oscilloscope, with resistor values from 3 KΩ down to 125 Ω. The delay in the current rising time was not detectable and the peak current can be increased to 1 A (at 125 Ω, 125 V).

The voltage across the sample capacitor C_2, during the charging cycle, is given by

$$v(t) = V_0 [1 - \exp(-t/RC_2)] \qquad \text{(A4)}$$

It shows that the voltage across the sample capacitor rises exponentially from zero to V_0 with a time constant of RC_2. The voltage–time waveform of the sample capacitor is shown in Fig. A3.

After a few time constants, the voltage of the sample capacitor is increased to V_0. To ensure that the sample capacitor can withstand such a voltage without breakdown, it usually soaks the capacitor at this voltage level for a few seconds then discharges the capacitor.

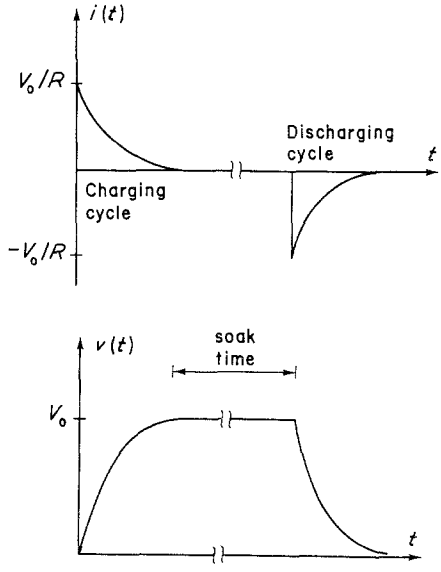

Figure A4.

The discharging current and voltage waveforms of the sample capacitor are the same as that of the charging cycle, except the polarities are inversed. The entire voltage and current waveforms of the sample capacitor are shown in Fig. A4.

In summary, the peak charging and discharging currents are determined by the associated resistors and the soaking voltage level V_0 and described by the equation

$$i_{max} = \frac{V_0}{R}$$

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